



Scaled CMOS Technology Reliability Users Guide

Mark White
Jet Propulsion Laboratory
Pasadena, California

Yuan Chen
Jet Propulsion Laboratory
Pasadena, California

Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California

JPL Publication 08-14 3/08



Scaled CMOS Technology Reliability Users Guide

NASA Electronic Parts and Packaging (NEPP) Program
Office of Safety and Mission Assurance

Mark White
Jet Propulsion Laboratory
Pasadena, California

Yuan Chen
Jet Propulsion Laboratory
Pasadena, California

NASA WBS: 939904.01.11.10
JPL Project Number: 102197
Task Number: 1.18.5

Jet Propulsion Laboratory
4800 Oak Grove Drive
Pasadena, CA 91109

<http://nepp.nasa.gov>

This research was carried out at the Jet Propulsion Laboratory, California Institute of Technology, and was sponsored by the National Aeronautics and Space Administration Electronic Parts and Packaging (NEPP) Program.

Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise, does not constitute or imply its endorsement by the United States Government or the Jet Propulsion Laboratory, California Institute of Technology.

Copyright 2008. California Institute of Technology. Government sponsorship acknowledged.

Table of Contents

| | |
|--|----|
| Scope..... | 1 |
| Section 1. Technology Scaling and Its Limits | 1 |
| 1.1 MOS scaling theory | 2 |
| 1.2 Moore's Law | 3 |
| 1.3 Scaling to its limits | 4 |
| Section 2. Technology Scaling Impact on Circuits..... | 6 |
| 2.1 Scaling impact on circuit performance | 6 |
| 2.2 Scaling impact on power consumption | 7 |
| 2.3 Scaling impact on circuit design..... | 8 |
| 2.3.1 Manage leakage power | 9 |
| 2.3.2 Manage uncertainty and variation..... | 9 |
| 2.3.3 Minimize single event upsets..... | 10 |
| Section 3. Technology Scaling Impact on Parts Reliability | 11 |
| 3.1 Scaling impact on parts burn-in | 11 |
| 3.2 Scaling impact on parts long term reliability | 12 |
| Section 4. Guidelines for Infusing Advanced CMOS Technology Parts in Space Applications | 15 |
| 4.1 Physics-of-Failure qualification..... | 18 |
| 4.2 Application-specific qualification..... | 18 |
| 4.3 Design-for-reliability approach..... | 19 |
| References..... | 20 |

Scope

This work is sponsored by the NASA Electronic Parts and Packaging (NEPP) Program. One of the objectives of this task is to prepare a body of knowledge guideline document summarizing the CMOS technology scaling impact on CMOS parts and parts reliability for space applications. Scaling impact on parts radiation sensitivity is not addressed in this report.

Section 1. Technology Scaling and Its Limits

Over the past three decades, CMOS technology scaling has been a primary driver of the electronics industry and has provided a path toward both denser and faster integration [1-13]. The transistors manufactured today are 20 times faster and occupy less than 1% of the area of those built 20 years ago. Predictions of size reduction limits have proven to elude the most insightful scientists and researchers. The predicted ‘limit’ has been dropping at nearly the same rate as the size of the transistors.

The number of devices per chip and the system performance has been improving exponentially over the last two decades. As the channel length is reduced, the performance improves, the power per switching event decreases, and the density improves. But the power density, total circuits per chip, and the total chip power consumption has been increasing. The need for more performance and integration has accelerated the scaling trends in almost every device parameter, such as lithography, effective channel length, gate dielectric thickness, supply voltage, device leakage, etc. Some of these parameters are approaching fundamental limits, and alternatives to the existing material and structures may need to be identified in order to continue scaling.

1.1 MOS scaling theory

During the early 1970s, both Mead [1] and Dennard [2] noted that the basic MOS transistor structure could be scaled to smaller physical dimensions. One could postulate a “scaling factor” of λ , the fractional size reduction from one generation to the next generation, and this scaling factor could then be directly applied to the structure and behavior of the MOS transistor in a straightforward multiplicative fashion. For example, a CMOS technology generation could have a minimum channel length L_{\min} , along with technology parameters such as the oxide thickness t_{ox} , the substrate doping N_A , the junction depth x_j , the power supply voltage V_{dd} , the threshold voltage V_{th} , etc. The basic “mapping” to the next process, $L_{\min} \rightarrow \lambda L_{\min}$, involved the concurrent mappings of $t_{\text{ox}} \rightarrow \lambda t_{\text{ox}}$, $N_A \rightarrow \lambda N_A$, $x_j \rightarrow \lambda x_j$, $V_{\text{dd}} \rightarrow \lambda V_{\text{dd}}$, $V_{\text{th}} \rightarrow \lambda V_{\text{th}}$, etc. Thus, the structure of the next generation process could be known beforehand, and the behavior of circuits in that next generation could be predicted in a straightforward fashion from the behavior in the present generation. The scaling theory developed by Mead and Dennard is solidly grounded in the basic physics and behavior of the MOS transistor. Scaling theory allows a “photocopy reduction” approach to feature size reduction in CMOS technology, and while the dimensions shrink, scaling theory causes the field strengths in the MOS transistor to remain the same across different process generations. Thus, the “original” form of scaling theory is constant field scaling.

Constant field scaling requires a reduction of the power supply voltage with each technology generation. In the 1980s, CMOS adopted the 5V power supply, which was compatible with the power supply of bipolar TTL logic. Constant field scaling was replaced with constant voltage scaling, and instead of remaining constant, the fields inside the device increased from generation to generation until the early 1990s, when excessive power dissipation and heating, gate dielectrics TDDB and channel hot carrier aging caused serious problems with the increasing electric field. As a result, constant field scaling was applied to technology scaling in the 1990s.

Constant field scaling requires that the threshold voltage be scaled in proportion to the feature size reduction. However, ultimately threshold voltage scaling is limited by the sub-threshold slope of the MOS transistor, which itself is limited by the thermal voltage kT/q , where the Boltzmann constant, k and the electron charge, q are fundamental constants of nature and cannot be changed. The choice of the threshold voltage in a particular technology is determined by the off-state current goal per transistor and the sub-threshold slope. With off-current requirements remaining the same (or even tightening) and the sub-threshold slope limited by basic physics, the difficulty with scaling the threshold voltage is clear. Because of this, the power supply voltage decreased corresponding with the constant field scaling, but the threshold voltage was unable to scale as aggressively. This situation worsens as feature sizes and power supply voltages continue to scale. This is a fundamental problem with further CMOS technology scaling.

1.2 Moore's Law

It was the realization of scaling theory and its usage in practice which has made possible the better-known "Moore's Law." Moore's Law is a phenomenological observation that the number of transistors on integrated circuits doubles every two years, as shown in Figure 1. It is intuitive that Moore's Law cannot be sustained forever. However, predictions of size reduction limits due to material or design constraints, or even the pace of size reduction, have proven to elude the most insightful scientists. The predicted 'limit' has been dropping at nearly the same rate as the size of the transistors.

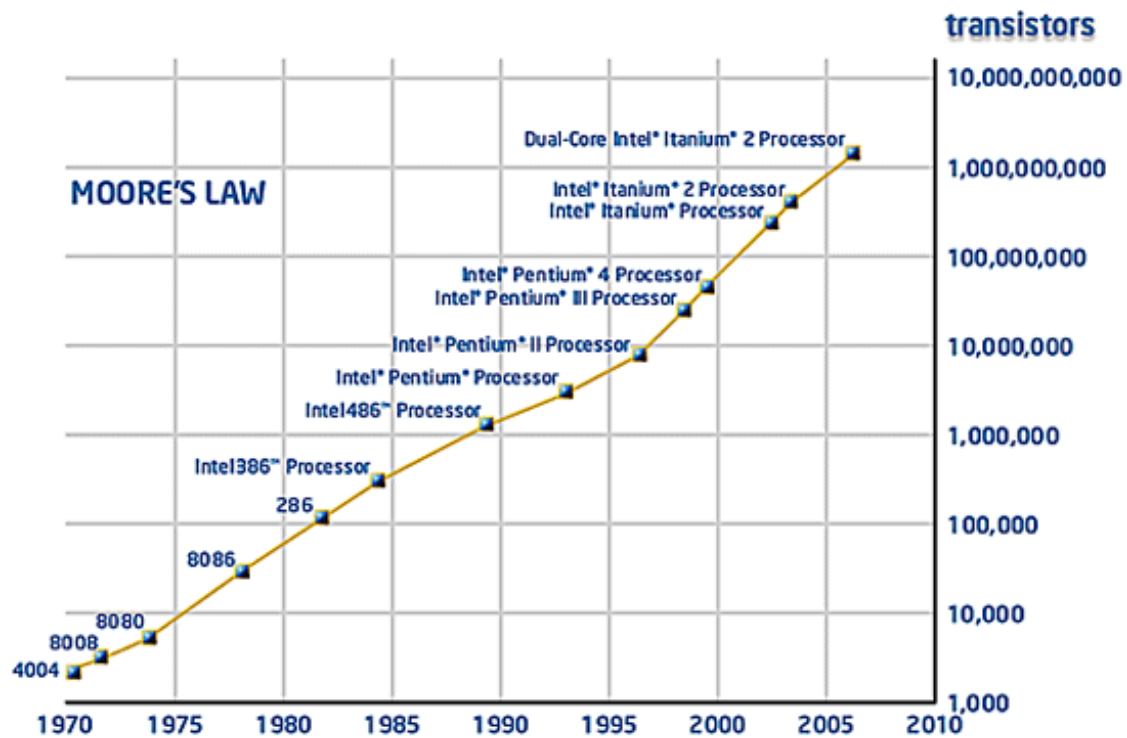


Figure 1. Moore's Law.

1.3 Scaling to its limits

There does not seem to be any fundamental physical limitation that would prevent Moore's Law from characterizing the trends of integrated circuits. However, sustaining this rate of progress is not a straightforward achievement [5].

Figure 2 shows the trends of power supply voltage, threshold voltage, and gate oxide thickness versus channel length for high performance CMOS logic technologies [6]. Sub-threshold non-scaling and standby power limitations bound the threshold voltage to a minimum of 0.2 V at the operating temperature. Thus, a significant reduction in performance gains is predicted below 1.5 V due to the fact that the threshold voltage decreases more slowly than the historical trend, leading to more aggressive device designs at higher electric fields.

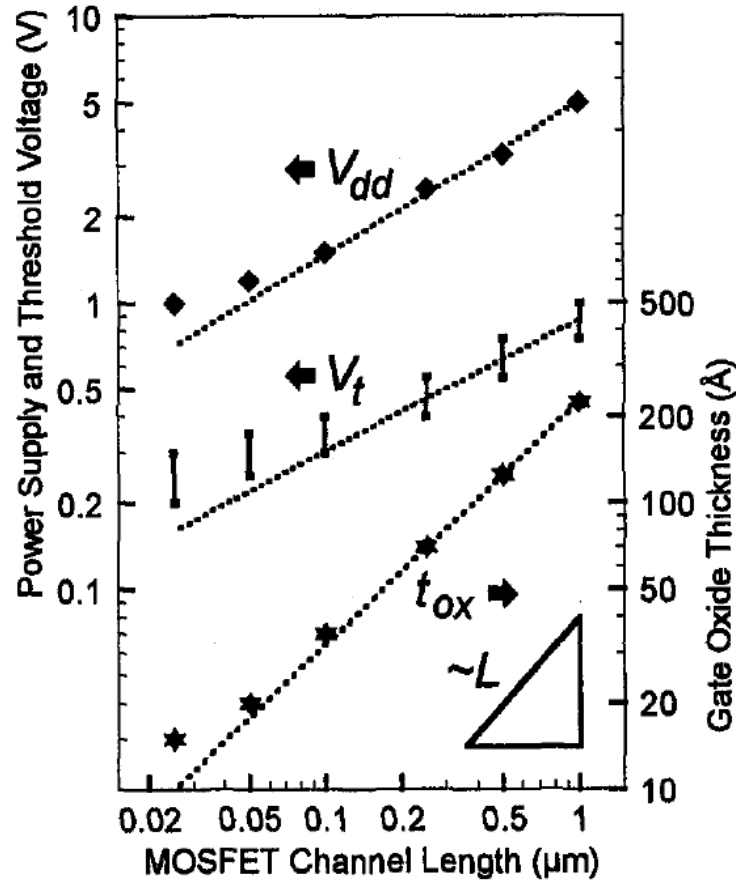


Figure 2. Trends of power supply voltage V_{dd} , threshold voltage V_{th} , and gate oxide thickness t_{ox} , versus channel length for CMOS logic technologies.

Further technology scaling requires major changes in many areas, including: 1) improved lithography techniques and non-optical exposure technologies; 2) improved transistor design to achieve higher performance with smaller dimensions; 3) migration from current bulk CMOS devices to novel materials and structures, including silicon-on-insulator, strained Si and novel dielectric materials; 4) circuit sensitivity to soft errors from radiation; 5) smaller wiring for on-chip interconnection of the circuits; 6) stable circuits; 7) more productive design automation tools; 8) denser memory cells, and 10) manageable capital costs. Metal gate and high-k gate dielectrics were introduced into production in 2007 to maintain technology scaling trends [14].

In addition, packaging technology needs to progress at a rate consistent with on-going CMOS technology scaling at sustainable cost/performance levels. This requires advances in I/O density, bandwidth, power distribution, and heat extraction. System architecture will also be required to maximize the performance gains achieved in advanced CMOS and packaging technologies.

Section 2. Technology Scaling Impact on Circuits

2.1 Scaling impact on circuit performance

Transistor scaling is the primary factor in achieving high-performance microprocessors and memories. Each 30% reduction in CMOS IC technology node scaling has [7, 19]: 1) reduced the gate delay by 30% allowing an increase in maximum clock frequency of 43%; 2) doubled the device density; 3) reduced the parasitic capacitance by 30%; and 4) reduced energy and active power per transition by 65% and 50%, respectively. Figure 3 shows CMOS performance, power density and circuit density trends, indicating a linear circuit performance as a result of technology scaling.

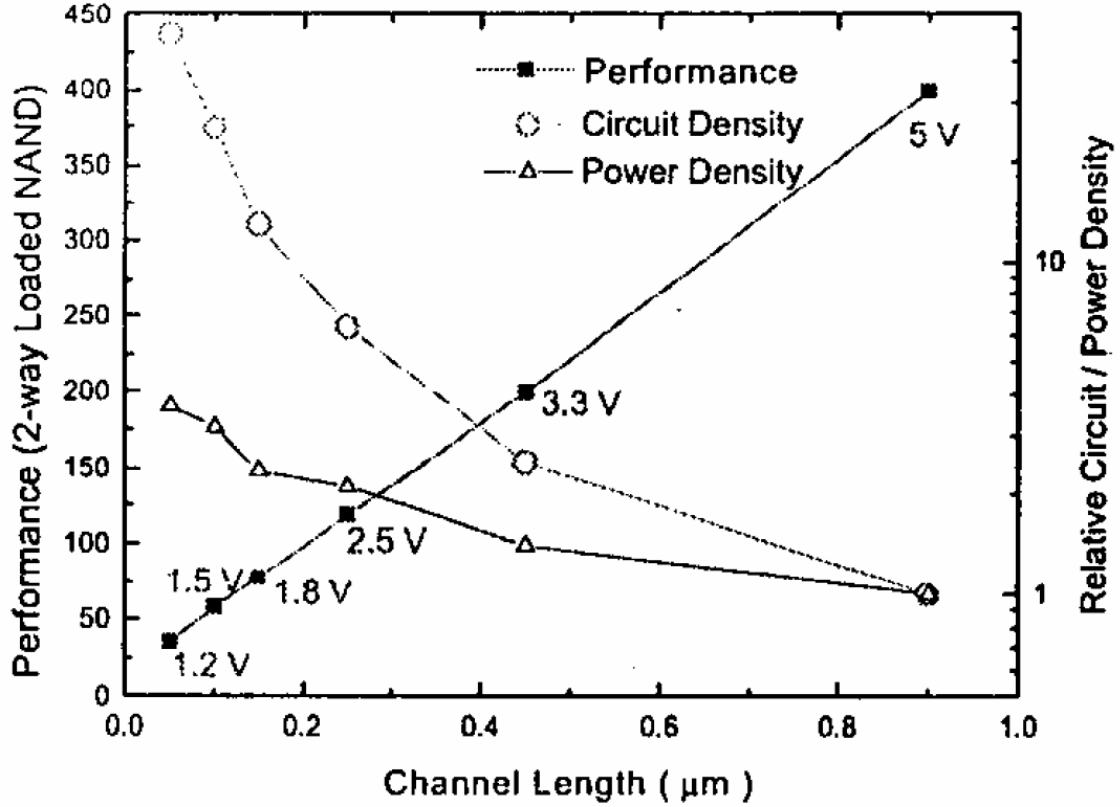


Figure 3. CMOS performance, power density and circuit density trends [7].

2.2 Scaling impact on power consumption

Dynamic power and leakage current are the major sources of power consumption in CMOS circuits. Leakage related power consumption has become more significant as threshold voltage scales with technology. There are several studies that deal with the impact of technology scaling in various aspects of CMOS VLSI design [5, 13, 15-17].

Figure 4 [16] illustrates how the dynamic and leakage power consumption vary across technologies, where P_{act} is the dynamic power consumption and P_{leak} is the leakage power consumption. The estimates have only captured the influence of sub-threshold currents since they are the dominant leakage mechanism. For sub-100nm technologies, temperature has a much greater impact on the leakage power consumption than the active

power consumption for the same technology. In addition, the leakage power consumption increases almost exponentially.

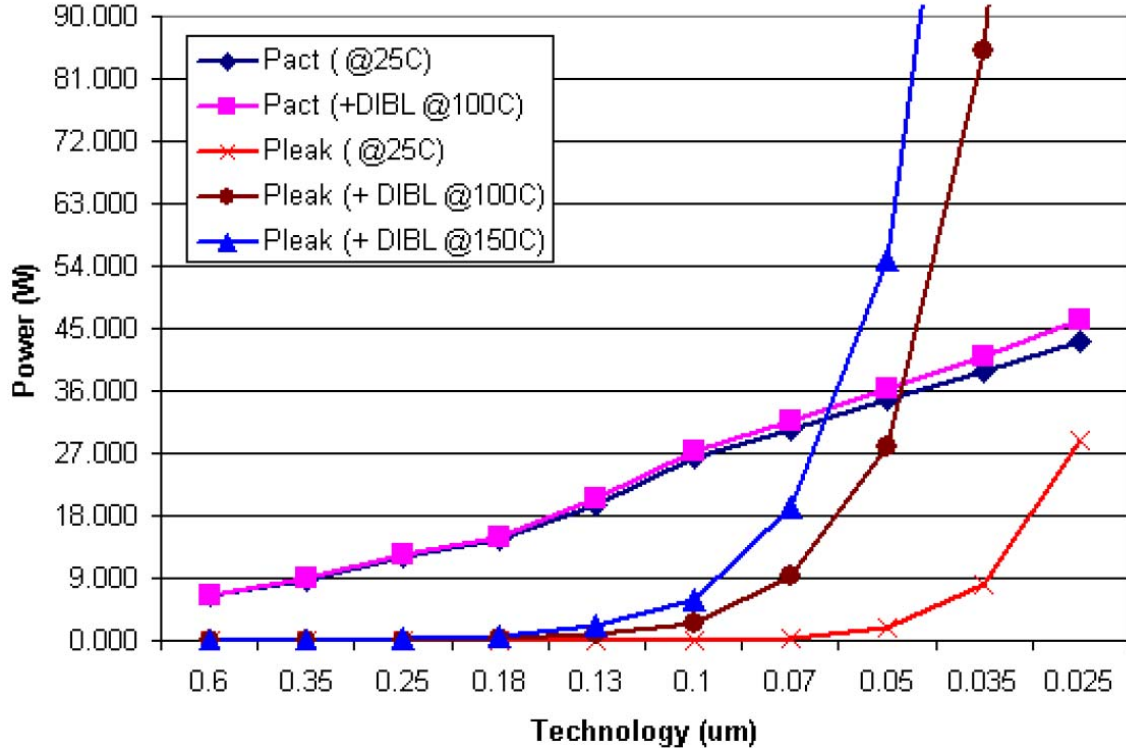


Figure 4. Active and leakage power for a constant die size.

2.3 Scaling impact on circuit design

With continuing aggressive technology scaling, it is increasingly difficult to sustain supply and threshold voltage scaling to provide the required performance increase, limit energy consumption, control power dissipation, and maintain reliability. These requirements pose several difficulties across a range of disciplines. On the technology front, the question arises whether we can continue along the traditional CMOS scaling path – reducing effective oxide thickness, improving channel mobility,

and minimizing parasitics. On the design front, researchers are exploring various circuit design techniques to deal with process variation, leakage and soft errors [7, 13].

2.3.1 Manage leakage power

For CMOS technologies beyond 90nm, leakage power is one of the most crucial design components which must be efficiently controlled in order to utilize the performance advantages of these technologies. It is important to analyze and control all components of leakage power, placing particular emphasis on sub-threshold and gate leakage power. A number of issues must be addressed, including low voltage circuit design under high intrinsic leakage, leakage monitoring and control, effective transistor stacking, multi-threshold CMOS, dynamic threshold CMOS, well biasing techniques, and design of low leakage data-paths and caches.

While supply voltage scaling becomes less effective in providing power savings as leakage power becomes larger due to scaling, it is suggested that the goal is to no longer have simply the highest performance, but instead have the highest performance within a particular power budget by considering the physical aspects of the design. In some cases, it may be possible to balance the benefit of using high threshold devices from a low leakage process running at the higher possible frequency at a full V_{dd} , as opposed to using faster but leakier devices which require more voltage scaling in order to reach the desired power budget.

2.3.2 Manage uncertainty and variation

Nanometer design technologies must work under tight operating margins, and are therefore highly susceptible to any process and environmental variability.

Traditional sources of variation due to circuit and environmental factors, such as cross capacitance, power supply integrity, multiple inputs switching, errors arising due to

tools and flows, etc., affect circuit performance significantly. To address environmental variation, it is important to build circuits that have well-distributed thermal properties, and to carefully design supply networks to provide reliable Vdd and ground levels throughout the chip.

With technology scaling, process variation has become more of a concern and has received an increased amount of attention from the design automation community. Several research efforts have addressed the issue of process variation and its impact on circuit performance [18-21]. A worst-case approach was first used to develop the closed form models for sensitivity due to different parameter variations for a clock tree [18], and was further developed to include interconnect and device variation impact on timing delay due to technology scaling [19]. The impact of systematic variation sources was then considered in [20]. Finally, an integrated variation analysis technique was developed in [21], which considers the effects of both systematic and random variation in both interconnect and devices simultaneously. The design community has realized that in order to address the process-induced variations and to ensure the final circuit reliability, instead of treating timing in a worst-case manner, as is conventionally done in static timing analysis, statistical techniques need to be employed that directly predict the percentage of circuits that are likely to meet a timing specification. The effects of uncertainties in process variables must be modeled using statistical techniques, and they must be utilized to determine variations in the performance parameters of a circuit.

2.3.3 Minimize single event upsets

Soft errors pose a major challenge for the design of memories and logic circuits in high-performance microprocessors in technologies beyond 90nm. Soft errors and single event upsets are gaining an increased amount of attention as technology scales. Measured data shows 8% soft error rate (SER) increase per bit per technology generation [22]. As the number of memory bits and sequential elements increase across generations, the soft

error problem is likely to become a serious barrier for advanced microprocessors. Historically, power-performance-area tradeoffs have been considered.

Scaling impact on radiation effects is beyond the scope of this document. It is important to emphasize, however, that there has been a demand to include the SER as another design parameter for circuit techniques for soft error tolerance in the industry for advanced CMOS circuits.

Section 3. Technology Scaling Impact on Parts Reliability

3.1 Scaling impact on parts burn-in

Power supply voltage in scaled technologies must be lowered for two main reasons [23]: 1) to reduce the device internal electric fields and 2) to reduce active power consumption since it is proportional to V_{DD}^2 . As V_{DD} scales, then V_{th} must also be scaled to maintain drain current overdrive to achieve higher performance. Lower V_{th} leads to higher off-state leakage current, which is the major problem with burn-in of scaled nanometer technologies.

The total power consumption of high-performance microprocessors increases with scaling. Off-state leakage current is a higher percentage of the total current at the sub-100-nm nodes under nominal conditions. The ratio of leakage to active power becomes worse under burn-in conditions and the dominant power consumption is from the off-state leakage. Typically, clock frequencies are kept in the tens of megahertz range during burn-in, resulting in a substantial reduction in active power. Conversely, the voltage and temperature stresses cause the off-state leakage to be the dominant power component.

Stress during burn-in accelerates the defect mechanisms responsible for early-life failures. Thermal and voltage stresses increase the junction temperature resulting in

accelerated aging. Elevated junction temperature, in turn, causes leakages to further increase. In many situations, this may result in positive feedback leading to thermal runaway. Such situations are more likely to occur as technology is scaled into the nanometer region. Thermal runaway increases the cost of burn-in dramatically. To avoid thermal runaway, it is crucial to understand and predict the junction temperature under normal and stress conditions. Junction temperature, in turn, is a function of ambient temperature, package to ambient thermal resistance, package thermal resistance, and static power dissipation. Considering these parameters, one can optimize the burn-in environment to minimize the probability of thermal runaway while maintaining the effectiveness of burn-in test.

3.2 Scaling impact on parts long term reliability

The major long-term reliability concerns include the wear-out mechanisms of time dependent dielectric breakdown (TDDB) of gate dielectrics, hot carrier injection (HCI), negative bias temperature instability (NBTI), electromigration (EM), and stress induced voiding (SIV). The physics and the reliability characterization and modeling of each mechanism have been the major research topics for the past three decades. There has been an abundant amount of research in this area, including [24].

Among the wear-out mechanisms, TDDB and NBTI seem to be the major reliability concerns as devices scale. The gate oxide has been scaled down to only a few atomic layers thick with significant tunneling leakage. While the gate leakage current may be at a negligible level compared with the on-state current of a device, it will first have an effect on the overall standby power. For a total active gate area of 0.1 cm^2 , chip standby power limits the maximum tolerable gate leakage current to approximately 1-10 A/cm², which occurs for gate oxides in the range of 15-18A [6].

Scaling impact of TDDB and NBTI on digital, analog and RF circuit reliability has been a hot topic during past years [25-35]. Either TDDB, NBTI, or both were found

to contribute to digital circuit speed degradation [25, 29], FPGA delay increase [32], SRAM minimum operating voltage V_{\min} shift measurement [31, 33, 34], RF circuit parametric drifts [27, 28], and analog circuit mismatch [26, 30]. It appears that SRAM minimum operating voltage V_{\min} shift due to TDDB and NBTI is one of the effects that has been tested and characterized most. For example, it is shown [33] that transistor shifts due to NBTI manifest themselves as population tails in the product's minimum operating voltage distribution. TDDB manifests itself as single-bit or logic failures that constitute a separate sub-population. NBTI failures are characterized by Log-normal statistics combined with a slower degradation rate, which is in contrast to TDDB failures that follow extreme-value statistics and exhibit a faster degradation rate. Most of the studies seem to indicate that the advanced technology parts may experience intrinsic or wear-out mechanisms induced circuit parametric shifts during operating life time, especially at higher operating voltages and temperature conditions.

Figure 5 [35] shows the normalized manufacturers' data on product level failure rate. It appears to suggest that technology scaling causes wear-out product failures much earlier than older technologies. At the same time, the constant failure rate, represented by the bottom portion of the bath-tub curve in Figure 5, also increases. This can be relatively easy to understand from the process induced defects point of view, which is illustrated in Figure 6. Depending on the defect size, location and distribution, it can be seen that technology scaling will no doubt increase the constant failure rate induced by the random defects, even with process improvements, which reduces defect size produced during semiconductor fabrication. This is because the same size of defects which are safe for older technologies may cause product yield and/or reliability concerns for advanced technologies simply because of the physical scaling. Figure 7 summarizes the failure rate trend as technology scales, i.e., constant failure rate increases with possible wear-out failures occurring earlier than expected.

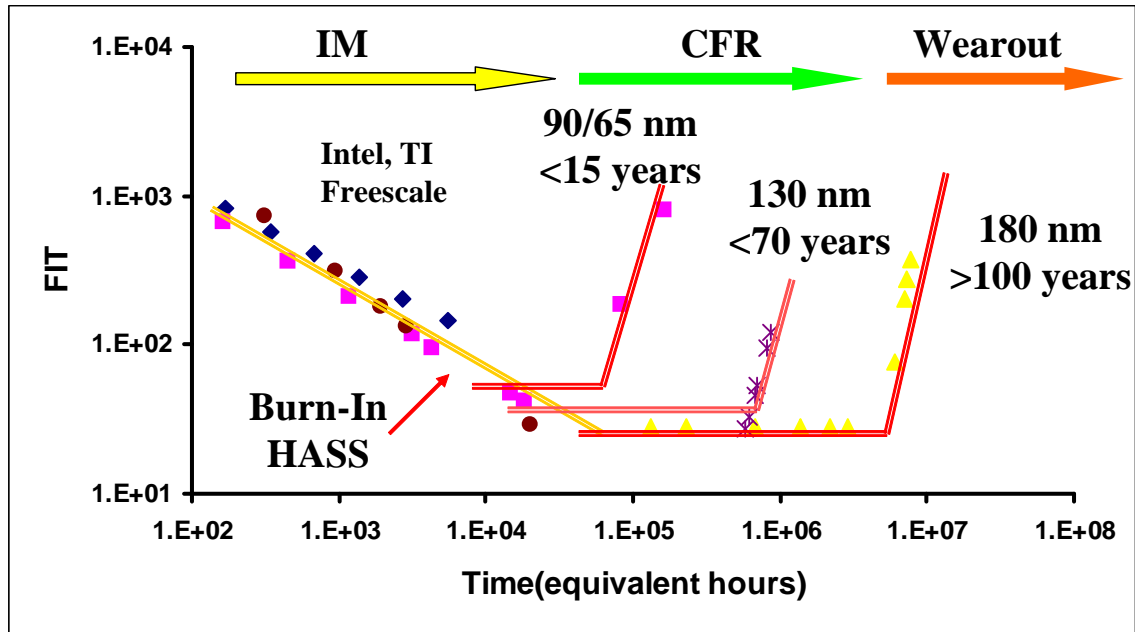


Figure 5. Normalized manufacturers' data on product level failure rate.

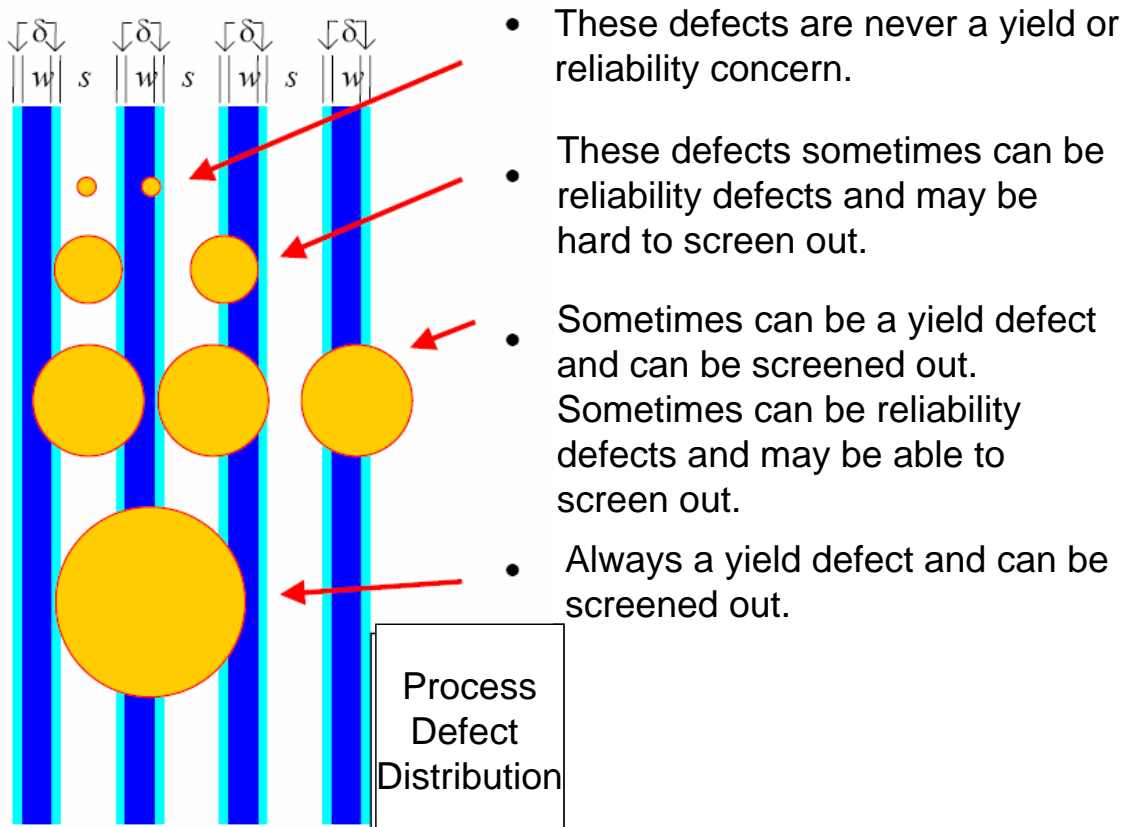


Figure 6. Illustration of process-induced defects: size, location and impact on semiconductor component yield and reliability.

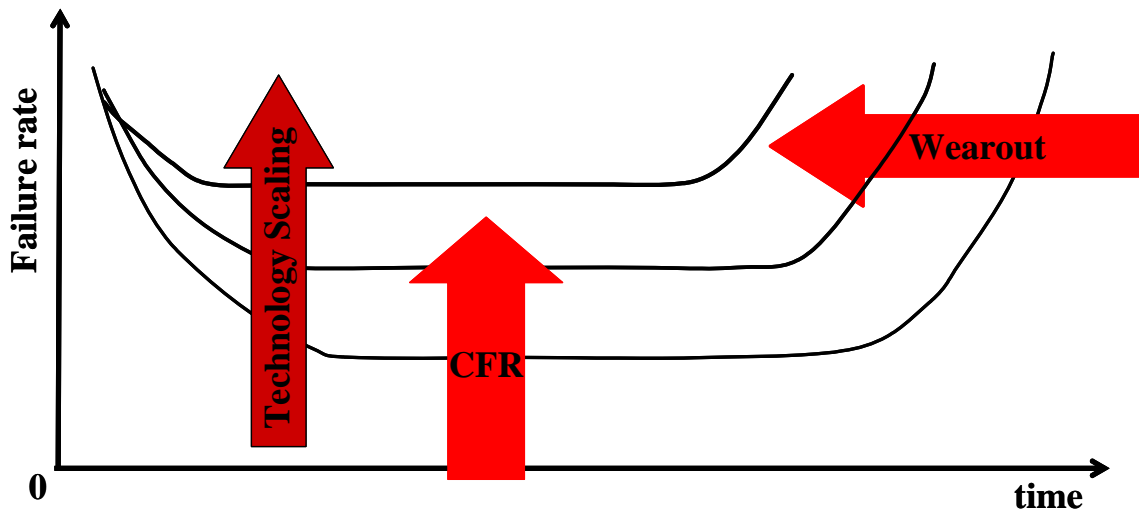


Figure 7. Product failure rate trend as technology scales. Constant failure rate increases with wear-out failures occurring earlier than expected.

Section 4. Guidelines for Infusing Advanced CMOS Technology Parts in Space Applications

International Technology Roadmap for Semiconductor (ITRS) predictions over the next few years will drive the semiconductor industry to reach both physical and material limitations as technology continues to scale. As a result, new materials, designs and processes will be employed to keep up with the performance demands of the industry. While target product lifetimes for mil-product have generally been ten years at maximum rated junction temperature, advanced CMOS technology microelectronics may be somewhat less due to technology scaling. Therefore, reliability uncertainty through the introduction of new materials, processes and architectures, coupled with the economic pressures to design for “reasonable life,” pose a concern to the hi-rel user of advanced CMOS technologies. These aspects, in addition to higher power and thermal densities, increase the risk of introducing new failure mechanisms and accelerating known failure mechanisms. With the increased failure rate of the advanced technologies, only

performing the qualification tests required by established military-standards will not be sufficient to qualify or understand the parts reliability to ensure mission success.

A comprehensive parts qualification and evaluation program is recommended for scaled CMOS technology components. The program may consist of three qualification and evaluation steps, i.e., physics-of-failure qualification, application specific qualification, and the design-for-reliability approach, which is summarized in Table 1. To achieve the goal of this comprehensive parts qualification and evaluation approach for advanced CMOS technology components, NASA will need to work closer with both component vendors and semiconductor foundries. As is illustrated in Figure 8, NASA should require both physics-of-failure based qualification information and product control information either through the semiconductor component vendors or directly from the semiconductor foundries. A much closer relationship between NASA, its vendors, and their foundries needs to be established to ensure the recommended comprehensive qualification and evaluation program to mitigate the risk of using advanced CMOS technology components in critical space flight applications.

Table 1. Comprehensive Parts Qualification and Evaluation Program
for Advanced CMOS Technologies

| Physics-of-Failure Qualification | | Application Specific Qualification | | Design-for-Reliability Approach | |
|----------------------------------|-----------------|------------------------------------|-------------------------|---------------------------------|---|
| Process and Technology Qual | | Application Conditions | | Parts Input | |
| | TDDDB | | Temperature profile | | Temperature profile |
| | NBTI | | Voltage range | | Voltage range |
| | HCA | | Radiation | | Radiation |
| | EM | Production Line Control | | | Parts statistics |
| | SIV | | SPC | | Burn-in impact on parts reliability |
| Product Qual | | | In-line monitor | | |
| | ESD | | Wafer-level | Board/System Input | |
| | Burn-in | Wafer/Die Selection | | | Parts failure criteria from board level |
| | Life Test | | Wafer level screening | | Parts degradation criteria from board level |
| | Yield | | Package level screening | | Board burn-in impact |
| | FTT estimate | Burn-in | | | |
| Packaging Qual | | | Technology dependent | Outcome | |
| | Bond pull | | Application dependent | | |
| | Thermal cycling | Life Test | | | Reliability by design |

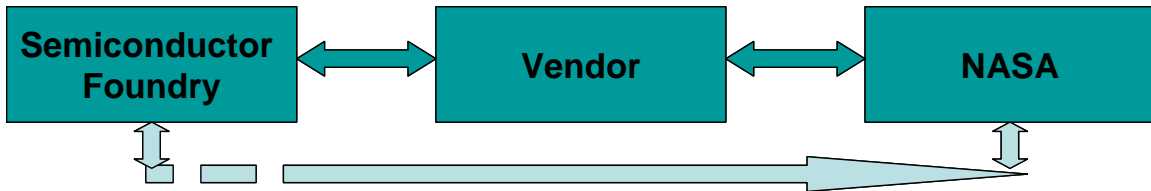


Figure 8. A much closer relationship between NASA, vendors and foundries needs to be established.

4.1 Physics-of-Failure qualification

The physics-of-failure approach has been used in the semiconductor industry for process and technology qualification, product qualification, and packaging qualification.

Process and technology qualification typically covers TDDB (Time Dependent Dielectrics Breakdown), NBTI (Negative Bias Temperature Instability), HCA (Hot Carrier Aging), EM (Electromigration), and SIV (Stress Induced Voids).

Product qualification generally includes ESD, burn-in, life test, yield analysis and failure rate (FIT) estimates.

Packaging qualification deals with bond pull strength, thermal cycling, etc. Thermal management and analysis is also determined.

The process and technology qualification, product qualification, and packaging qualification are performed by semiconductor foundries and typically follow JEDEC standards [36-42].

4.2 Application-specific qualification

Application-specific qualification should consider application conditions including the temperature profile, voltage range and radiation environment the parts are expected to endure during the specific mission. Production line control information, i.e., statistical process control parametrics, in-line monitoring, wafer-level parametrics, and both wafer level and package level screening, should be reviewed for wafer and/or parts selection. Burn-in should be technology and application dependent, and life testing should be performed for further reliability confirmation.

Burn-in at temperature ranges of 125°C to 150°C for an extended period of time between 96 hours to 240 hours has been specified and required in Mil-Std-883 for high-reliability electronic parts in space applications. For advanced technologies, burn-in optimization for yield and reliability is of crucial significance due to a larger number of design and technology variables. At the same time, technology scaling yields smaller transistor geometries as well as increased sub-threshold and gate leakages. This results in higher junction temperatures and device self-heating. The elevated junction temperature, in turn, causes leakages to increase further and may result in positive feedback leading to thermal runaway. Therefore, thermal runaway avoidance needs to be addressed during burn-in. This is especially true when the parts are to be burned-in above the standard operating temperature. In addition, temperature derating requirements must be revisited to ensure that an acceptable thermal margin exists for space parts qualification. In some circumstances, individual chip level burn-in optimization may be necessary in order to provide an optimum burn-in environment for each chip, and the deep-submicron devices may require advanced packaging and even liquid cooling techniques to lower the junction to ambient thermal resistance. The burn-in of sub-90nm parts requires a re-evaluation of standard screening procedures and an understanding of the part thermal management so that they are suitably applied and will meet mission requirements.

4.3 Design-for-reliability approach

Design-for-reliability approach is the third step to ensure mission success. Both parts and board/system level information need to be integrated together for mission reliability qualification, evaluation and mission assurance. Key parts related information includes temperature profile, voltage range/duty cycle, radiation environment, parts parametric and reliability statistics, and burn-in conditions and their impact on parts reliability. Key board and/or system level information includes parts failure and degradation criteria on the boards and systems, and the potential parts reliability impact from board level burn-in. The design-for-reliability methodology has been developed for

extreme space applications with case studies [43-45] and needs to be further developed and applied to advanced CMOS technology components.

References

1. C. Mead, "Fundamental limitations in microelectronics – I. MOS technology," *Solid State Electronics*, vol. 15, pp. 819–829, 1972.
2. R. H. Dennard, F. H. Gaensslen, H-N, Yu, V.I. Rideout, E. Bassous, and A. R. LeBlanc, "Design of ion-implanted MOSFET's with very small physical dimensions," *IEEE Journal of Solid-State Circuits*, SC-9, pp.256–268, 1974.
3. H. Iwai, "CMOS Scaling towards its Limits," *IEEE*, pp. 31–34, 1998.
4. R.D. Isaac, "Reaching the Limits of CMOS Technology," *IEEE*, pp. 3, 1998.
5. S. Borkar, "Design Challenges of Technology Scaling," *IEEE Micro*, pp. 23–29, 1999.
6. Y. Taur, "CMOS Scaling Beyond 0.1 μ m: How Far Can it Go," *VLSI-TSA*, pp. 6–9, 1999.
7. G. G. Shahidi, "Challenges of CMOS scaling at below 0.1 μ m," *The 12th International Conference on Microelectronics*, October 31–November 2, 2000.
8. "L. Chang, et al., "Moore's Law Lives on," *IEEE Circuits and Devices Magazine*, pp. 35–42, January 2003.
9. D. Foty, et al., "CMOS Scaling Theory – Why Our Theory of Everything Still Works and What that Means for the Future," *IEEE*, 2004.
10. T. Skotnicki, et al., "The End of CMOS Scaling," *IEEE Circuits and Devices Magazine*, pp. 16–26, January 2005.
11. K. Lee, et al., "The Impact of Semiconductor Technology Scaling on CMOS RF and Digital Circuits for Wireless Application," *IEEE Transactions on Electron Devices*, Vol. 52, No.7, July 2005.
12. T. Chen, et al., "Overcoming Research Challenges for CMOS Scaling: Industry Directions," *IEEE*, 2006.
13. R. Puri, T. Karnik, R. Joshi, "Technology Impacts on sub-90nm CMOS Circuit Design & Design methodologies," *Proceedings of the 19th International Conference on VLSI Design*, 2006.
14. Intel news release, 2007.
15. D. Sylvester, et al., "Future Performance Challenges in Nanometer Design," *Proceedings of the 38th DAC*, pp. 3–8.
16. D. Duarte, et al., "Impact of Scaling on the Effectiveness of Dynamic Power Reduction Schemes," *Proceedings of the 2002 IEEE International Conference on Computer Design: VLSI in Computers and Processors*, 2002.
17. R. Viswanath, et al., "Thermal Performance Challenges from Silicon to Systems," *Intel Technology Journal*, 3rd quarter, 2000.
18. P. Zarkesh-Ha et al., "Chip Clock Distribution Networks," *Proc. IITC*, June 1999
19. S. Nassif, "Design for Variability in DSM Technologies," *Proc ISQED*, 2000.
20. V. Mehrotra et al., "Modeling the Effects of Manufacturing Variation on High-speed Microprocessor Interconnect Performance," *Proceedings of IEDM*, December 1998.

21. V. Mehrotra et al., "Technology Scaling Impact of Variation on Clock Skew and Interconnect Delay," *IEEE*, 2001.
22. P. Hazucha et al., "Neutron Soft Error Rate Measurements in a 90-nm CMOS Process and Scaling Trends in S/spl mu/m to 90-nm Generation," *Proceedings of IEDM*, December 2003.
23. A. Vassighi, et al., "CMOS IC Technology Scaling and Its Impact on Burn-in," *IEEE Transactions on Device and Materials Reliability*, Vol. 4, No. 2, pp. 208–221, June 2004.
24. M. White, et al., "Microelectronics Reliability: Physics-of-Failure Based Modeling and Lifetime Evaluation," JPL Publication 08-5 2/08, 2008.
25. IEDM.
26. Y. Chen, et al, "Stress-Induced MOSFET Mismatch for Analog Circuit," *IEEE International Integrated Reliability Workshop*, 2001.
27. H. Yang, et al, "Effect of Gate Oxide Breakdown on RF Device and Circuit Performance," *IEEE International Reliability and Physics Symposium*, 2003.
28. C. Schlunder, et al, "On the Degradation of P-MOSFETS in Analog and RF Circuit Under Inhomogeneous Negative Bias Temperature Stress," *International Reliability and Physics Symposium*, 2003.
29. R. Rodriguez, et al, "Modeling and Experimental Verification of the Effect of Gate Oxide Breakdown on CMOS Inverters," *International Reliability and Physics Symposium*, 2003.
30. M. Agostinelli, et al, "PMOS NBTI-Induced Circuit Mismatch in Advanced Technologies," *IEEE International Reliability and Physics Symposium*, 2004.
31. J. Maiz, "Reliability Challenges: Preventing Them from Becoming Limiters to Technology Scaling," *IEEE International Integrated Reliability Workshop*, 2006.
32. A. Krishnan, "NBTI: Process, Device, and Circuits," *IEEE International Reliability Physics Symposium*, 2005.
33. A. Haggag, et al., "Realistic Projection of Product Fails from NBTI and TDDB," *IEEE International Reliability Physics Symposium*, pp. 541–544, 2006.
34. A. Haggag, et al., "Understanding SRAM High-Temperature-Operating-Life NBTI: Statistics and Permanent vs Recoverable Damage," *IEEE International Reliability Physics Symposium*, pp. 452–456, 2007.
35. J. Bernstein, AVSI Quarter Report, 2006.
36. JP001-01, "Foundry Process Qualification Guidelines," JEDEC, 2004.
37. JESD92, "Procedure for Characterizing Time-Dependent Dielectric Breakdown of Ultra-Thin Gate Dielectrics," JEDEC, 2003.
38. JESD61, "Isothermal Electromigration Test Procedures," JEDEC, 1997.
39. JESD63, "Standard Method for Calculating the Electromigration Model Parameters for Current Density and Temperature," JEDEC, 1998.
40. JESD28-A, "A Procedure for Measuring N-Channel MOSFET Hot-Carrier-Induced Degradation under DC Stress," JEDEC, 2001.
41. JESD60A, "A Procedure for Measuring N-Channel MOSFET Hot-Carrier-Induced Degradation at Maximum Gate Current under DC Stress," JEDEC, 2004.
42. JEP139, "Constant Temperature Aging to Characterize Aluminum Interconnect Metallization for Stress-Induced Voiding," JEDEC, 2000.

43. Y. Chen, et al, "Approach to Extrapolating Reliability of Circuit Operating in a Varying and Low Temperature Range," *IEEE International Reliability Physics Symposium*, 2006.
44. Y. Chen, et al, "Design for ASIC Reliability for Low Temperature Applications," *IEEE Transaction on Device and Material Reliability*, June 2006.
45. Y. Chen, et al, "A Case Study: Design for Reliability for a Rail-to-Rail Operational Amplifier for Wide Temperature Range Operation for Mars Missions," *IEEE International Reliability Physics Symposium*, 2008.

| REPORT DOCUMENTATION PAGE | | | | Form Approved OMB No. 0704-0188 | |
|---|------------------|-----------------------------------|--|-------------------------------------|---|
| <p>The public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Department of Defense, Washington Headquarters Services, Directorate for Information Operations and Reports (0704-0188), 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302. Respondents should be aware that notwithstanding any other provision of law, no person shall be subject to any penalty for failing to comply with a collection of information if it does not display a currently valid OMB control number.</p> <p>PLEASE DO NOT RETURN YOUR FORM TO THE ABOVE ADDRESS.</p> | | | | | |
| 1. REPORT DATE (DD-MM-YYYY) 20-03-2008 | | 2. REPORT TYPE JPL Publication | | 3. DATES COVERED (From - To) N/A | |
| 4. TITLE AND SUBTITLE Scaled CMOS Technology Reliability Users Guide | | | 5a. CONTRACT NUMBER NAS7-03001 | | |
| | | | 5b. GRANT NUMBER | | |
| | | | 5c. PROGRAM ELEMENT NUMBER | | |
| 6. AUTHOR(S) White, Mark; and Chen, Yuan | | | 5d. PROJECT NUMBER 102197 | | |
| | | | 5e. TASK NUMBER 1.18.5 | | |
| | | | 5f. WORK UNIT NUMBER | | |
| 7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) Jet Propulsion Laboratory California Institute of Technology 4800 Oak Grove Drive Pasadena, CA 91009 | | | 8. PERFORMING ORGANIZATION REPORT NUMBER JPL Publication 08-14 | | |
| 9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES) National Aeronautics and Space Administration Washington, DC 20546-0001 | | | 10. SPONSORING/MONITOR'S ACRONYM(S) NASA NEPP | | |
| | | | 11. SPONSORING/MONITORING REPORT NUMBER 0 | | |
| 12. DISTRIBUTION/AVAILABILITY STATEMENT Unclassified—Unlimited | | | | | |
| Subject Category Engineering-33 | | | | | |
| Availability: NASA CASI (301) 621-0390 Distribution: Nonstandard | | | | | |
| 13. SUPPLEMENTARY NOTES | | | | | |
| 14. ABSTRACT This users guide provides an overview of technology scaling, technology scaling impact on circuits, technology scaling impact on parts reliability, and guidelines for infusing advanced CMOS technologies in space applications. | | | | | |
| 15. SUBJECT TERMS Scaled CMOS, Scaling, Reliability | | | | | |
| 16. SECURITY CLASSIFICATION OF: | | | 17. LIMITATION OF ABSTRACT UU | 18. NUMBER OF PAGES 27 | 19a. NAME OF RESPONSIBLE PERSON STI Help Desk at help@sti.nasa.gov |
| a. REPORT U | b. ABSTRACT U | c. THIS PAGE U | | | 19b. TELEPHONE NUMBER (Include area code) (301) 621-0390 |